REMARKS

The claims remaining in the present application are Claims 1-11, 13, and 21-25. Claim 8 has been amended. Claim 10 has been cancelled, without prejudice. No new matter has been added as a result of these claim amendments.

ALLOWED CLAIMS

Claims 22-25 are allowed by the Examiner. The Applicants thank the Examiner for allowing these claims.

ALLOWABLE CLAIMS

Claims 5-7 and 9-13 are indicated as allowable by the Examiner if re-written in independent form to incorporate all limitations from base and intervening claims. The Applicants thank the Examiner for indicating this allowable subject matter.

Claims 5-7 and 9-13 are discussed in the rejection to independent Claims 1 and 8.

CLAIM REJECTIONS

Claims 1-4

Claims 1-4 are rejected under the judicially created doctrine of double patenting over Claims 1-3 and 10 of U.S. Patent No 6,490,712. The

Applicants have filed herewith a terminal disclaimer obviating the double patenting rejection. Therefore, Claims 1-4 are respectfully believed to be allowable over the prior art.

Claims 5-7 and 21 depend from Claim 1, which is respectfully believed to be allowable for the foregoing reasons. Therefore, Claims 5-7 and 21 are respectfully believed to be allowable by virtue of dependency from Claim 1.

Claim 8

Claim 8 is rejected under 35 U.S.C. §102 as being anticipated by Varadarajan et al. U.S. Patent No. 5,838,583 (hereinafter, Varadarajan). The rejection is respectfully traversed for the following reasons.

Amended Independent Claim 8 reads:

> A computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:
>
> a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses in an address space of a memory operable to store configuration bits for programming a programmable logic device;
>
> b) accessing a data structure specifying an order in which said plurality of addresses are traversed when loading said configuration bits into said programmable logic device;
>
> c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b) and information in the data structure comprising the plurality of logical names corresponding to the plurality of addresses, said ordering comprising determining whether there is a configuration bit at addresses in the address space based on information in the data structure comprising the plurality of logical names; and

d) automatically storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading said configuration bits into said programmable logic device.

Claim 8 has been amended to incorporate limitations from Claim 10, which has been indicated by the Examiner as allowable for reasons above. Therefore, Applicants respectfully believe that amended independent Claim 8 is allowable over the prior art.

Claims 9, 11 and 13 depend from Claim 8. As Claim 8 is respectfully believed to be allowable, allowance of Claims 9-11 and 13 is respectfully solicited.

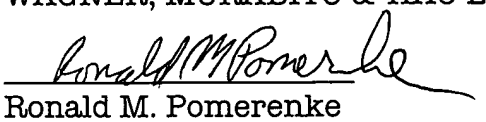
CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected Claims is requested. Based on the arguments and amendments presented above, it is respectfully submitted that Claims 1-9, 11, 13, and 21-25 overcome the rejections of record. Therefore, allowance of Claims 1-9, 11, 13, and 21-25 is earnestly solicited.

Should the Examiner have a question regarding the instant amendment and remarks, the Applicants invites the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 10/1, 2004



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